Application Note 2713
Switching Frame Mode in Live T1 Systems

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INTRODUCTION

When using or testing T1 systems, it may be possible to switch between the D4 and ESF framing patterns during live operation. Under certain circumstances this may cause problems in the system and should be avoided if possible. The reason is that both the ESF and D4 framing patterns are similar enough to cause problems with synchronization. One specific case is when the receiver is in ESF mode and the transmitter is switched from ESF to D4 mode. If the receiver was synchronized prior to the switch, there is a 1 in 6 chance the receiver will not declare loss of synchronization.

T1 FRAMING PATTERNS

In D4 mode, all the framing pattern bits are used for synchronization. The bits are divided into two sets known as Ft and Fs bits. The Ft bits are used to indicate the start of the multiframe and the Fs bits are used to indicate the signaling frames. The D4 multiframe consists 12 frames with the following framing pattern:

Full D4 Framing Pattern:
1000 1101 1100 ...

In ESF mode, only one-fourth of the framing pattern bits are used for synchronization. Every fourth bit of the framing pattern is a FPS bit used for synchronization; the remaining bits are for the facilities data link (FDL) and the CRC6 checksum. The ESF multiframe consists of 24 frames with the following framing pattern ("d" indicates the FDL bits, "c" indicates the CRC6 bits, and "0" or "1" indicate the FPS bits):

Full ESF Framing Pattern:
dcd0 dcd0 dcd1 dcd0 dcd1 dcd1 ...

T1 FRAMING PATTERN COMPARISON

Table 1 shows the similarities in the D4 and ESF framing patterns. Because the D4 framing pattern is 12 bits long, it is repeated twice on the first line for comparison to the 24-bit ESF framing pattern. The remaining lines are the ESF framing pattern shifted left one bit at a time to create the 24 possible comparisons. When comparing the D4 framing pattern against the ESF framing pattern, it is only necessary to compare the FPS bits. While most of the patterns only match one or three bits, patterns 3, 5, 15, and 17 match five of the six synchronization bits.

In normal operation, a certain number of bit errors are expected and need to be tolerated so that the line can remain operational. This includes errors in the synchronization bits. To conform to telecom standards, many T1 devices allow an out-of-frame (OOF) condition to be declared on two errors in 4, 5, or 6 frame bits. However, there are no provisions for one error in 6 frame bits, produced by the above-mentioned patterns. There are three possible methods to detect this condition. The software can use the frame bit-error indicator, the FPS pattern error counter, or the CRC6 error counter. The frame bit-error (FBE) condition will be set once every 6 frames. The multiframes out-of-sync counter can count errors in the FPS pattern. Since the counter is updated every second and every FPS pattern is erred, the counter will always read 333 or 334. The path-code violation counter can count errors in the CRC6 codewords. Since this counter is also updated every second and no CRC6 codewords are present, the counter will always read 333 or 334. Once the software is alerted to one or more of these events, a resynchronization can be forced, which causes the device to lose synchronization. The initial synchronization will not lock if there are any bit errors in the synchronization pattern.

It should be noted that this situation is unlikely to happen in the field. Fielded equipment is usually set for one mode of operation and rarely changed.

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Table 1. D4 and ESF Framing Pattern Comparison

FRAME TYPE	PATTERN NUMBER	PATTERN BITS	MATCHING BITS
D4	—	1000 1101 1100 1000 1101 1100	—
—	—	—	—
ESF	01	dcd0 dcd0 dcd1 dcd0 dcd1 dcd1	3
ESF	02	cd0d cd0d cd1d cd0d cd1d cd1d	3
ESF	03	d0dc d0dc d1dc d0dc d1dc d1dc	5
ESF	04	0dcd 0dcd 1dcd 0dcd 1dcd 1dcd	3
ESF	05	dcd0 dcd1 dcd0 dcd1 dcd1 dcd0	5
ESF	06	cd0d cd1d cd0d cd1d cd1d cd0d	3
ESF	07	d0dc d1dc d0dc d1dc d1dc d0dc	3
ESF	08	0dcd 1dcd 0dcd 1dcd 1dcd 0dcd	3
ESF	09	dcd1 dcd0 dcd1 dcd1 dcd0 dcd0	1
ESF	10	cd1d cd0d cd1d cd1d cd0d cd0d	3
ESF	11	d1dc d0dc d1dc d1dc d0dc d0dc	1
ESF	12	1dcd 0dcd 1dcd 1dcd 0dcd 0dcd	3
—	—	—	—
ESF	13	dcd0 dcd1 dcd1 dcd0 dcd0 dcd1	3
ESF	14	cd0d cd1d cd1d cd0d cd0d cd1d	3
ESF	15	d0dc d1dc d1dc d0dc d0dc d1dc	5
ESF	16	0dcd 1dcd 1dcd 0dcd 0dcd 1dcd	3
ESF	17	dcd1 dcd1 dcd0 dcd0 dcd1 dcd0	5
ESF	18	cd1d cd1d cd0d cd0d cd1d cd0d	3
ESF	19	d1dc d1dc d0dc d0dc d1dc d0dc	3
ESF	20	1dcd 1dcd 0dcd 0dcd 1dcd 0dcd	3
ESF	21	dcd1 dcd0 dcd0 dcd1 dcd0 dcd1	1
ESF	22	cd1d cd0d cd0d cd1d cd0d cd1d	3
ESF	23	d1dc d0dc d0dc d1dc d0dc d1dc	1
ESF	24	1dcd 0dcd 0dcd 1dcd 0dcd 1dcd	3